

Appl. No. 09/783,187

Amdt. Dated June 23, 2004

Reply to Office Action of April 2, 2004

REMARKS/ARGUMENTS

Reconsideration of the application is requested.

Claims 8-15 are in the application. Claims 1-7 were withdrawn from examination and previously canceled. Claims 8 and 12 have been amended. Dependent claim 15 has been added.

Support for the feature in new dependent claim 15 is on page 7, lines 22-26 of the instant specification.

It is noted that on page 1 (item 4) of the above-identified Office Action, the Examiner has indicated that claims 8-10 are pending in the subject application. However, applicants' record shows that claims 8-14 are pending in the subject application. Claims 1-14 were originally filed in the subject application. In the Examiner's Amendment dated May 6, 2003, the Examiner canceled claims 1-7, which were withdrawn from examination, being directed to a non-elected invention. Thereafter, claims 8-14 remained in the subject application. The reply post card (copy attached) for the originally filed subject application indicates that the instant application contained 27 pages. The claims appear on pages 23-26 and claims 11-14 appear on page 26 (copy enclosed) of the original application. It appears that the Patent Office inadvertently

Appl. No. 09/783,187

Amdt. Dated June 23, 2004

Reply to Office Action of April 2, 2004

failed to include claims 11-14 in the official application file and in the published version of the instant application (please refer to the Updated Filing Receipt Confirmation 2119 which indicates a total of 10 claims, instead of the correct number of 14 total claims). Notwithstanding the foregoing, claims 11-14 are shown in the Claim Amendments section of the instant amendment.

In the first item on page 2 of the above-identified Office Action, the Examiner has withdrawn the allowability of claims 8-10 in view of the newly-cited reference of Krautschneider et al. The Patent Office withdrew the instant application from issue in the Notice of Withdrawal from Issue Under 37 C.F.R. 1.313 enclosed with the aforesaid Office Action.

In the third item on page 2 of the above-identified Office Action, claims 8-10 have been rejected as being anticipated by Krautschneider et al. (U.S. 5,471,417) (hereinafter "Krautschneider") under 35 U.S.C. § 102(b).

The rejection has been noted and the claims have been amended in an effort to even more clearly define the invention of the instant application. Support for this change is found, for example, on page 4, lines 10-14 of the instant specification.

Appl. No. 09/783,187

Amdt. Dated June 23, 2004

Reply to Office Action of April 2, 2004

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

Claim 1 calls for, *inter alia*, a memory configuration, having:

a read/store control apparatus connected to the memory cells for controlling one of reading a state from one of the ferroelectric transistors and storing a state to the one of the ferroelectric transistors; and

the read/store control apparatus being configured such that the state is one of read from the one of the ferroelectric transistors and stored in the one of the ferroelectric transistors, and such that a threshold voltage of at least a further one of the ferroelectric transistors in the memory matrix is increased by applying a drain-substrate voltage.

(emphasis added)

Independent claim 8, as amended, now clarifies in that a threshold voltage of at least a further one of the ferroelectric transistors in a memory matrix of a memory configuration is increased by applying a drain-substrate voltage.

Krautschneider discloses that, in order to prevent the ferroelectric layer in an unselected memory cell from becoming

Appl. No. 09/783,187

Amdt. Dated June 23, 2004

Reply to Office Action of April 2, 2004

repolarized in a memory cell arrangement when a selected memory cell is repolarized, the electric field of the ferroelectric layer of the unselected memory cells are reduced. However, according to Krautschneider, this is achieved, according to one embodiment, by increasing the potential present at the source region and at the drain region to half the value which is present at the word line (see column 3, lines 12-26 of Krautschneider) or alternatively, according to a second embodiment, by applying a voltage corresponding to half the value of the voltage applied to the word line at the substrate below a ferroelectric layer in the memory cells (see column 3, lines 27-49 and column 7, lines 14-24 of Krautschneider).

Krautschneider does not show a configuration for increasing the threshold voltage of the unselected ferroelectric transistors by applying a drain-substrate voltage to the unselected ferroelectric transistors.

According to the present invention, applying a drain-substrate voltage to a ferroelectric transistor results in the formation of a plateau in the hysteresis loop of the ferroelectric transistor which defines the ferroelectric polarization profile. This plateau is sufficient to prevent a change to an indistinguishable polarization state as a result of a change

Appl. No. 09/783,187

Amdt. Dated June 23, 2004

Reply to Office Action of April 2, 2004

to the gate voltage, which is produced by reading or storing a state from or in an adjacent ferroelectric transistor.

Krautschneider does not even suggest formation of a plateau in the hysteresis loop of a ferroelectric transistor as recited in new dependent claim 15.

Since Krautschneider does not disclose the formation of the plateau by applying a substrate-drain voltage to a ferroelectric transistor and because of the advantages afforded by the present claimed invention, in particular due to the simple way of preventing the undesired repolarization of an unselected memory cell, independent claim 8 and dependent claim 15 are believed to be patentably distinguishable over Krautschneider.

Clearly, Krautschneider does not show "said read/store control apparatus being configured ... such that a threshold voltage of at least a further one of said ferroelectric transistors in said memory matrix is increased by applying a drain-substrate voltage" as recited in claim 8 of the instant application.

Nor does Krautschneider show that "the applied drain-substrate voltage forms a plateau in a hysteresis loop of said further one

Appl. No. 09/783,187

Amdt. Dated June 23, 2004

Reply to Office Action of April 2, 2004

of said ferroelectric transistors to define a ferroelectric polarization profile" as recited in dependent claim 15 of the instant application.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claim 8. Claim 8 is, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claim 8.

In view of the foregoing, reconsideration and allowance of claims 8-14 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out.

If an extension of time for this paper is required, petition for extension is herewith made.

Appl. No. 09/783,187

Amdt. Dated June 23, 2004

Reply to Office Action of April 2, 2004

Please charge any other fees that might be due with respect to

Sections 1.16 and 1.17 to the Deposit Account of Lerner and

Greenberg, P.A., No. 12-1099.

Respectfully submitted,

LAURENCE A. GREENBERG
REG. NO. 29,308



For Applicants

FDP/tk

June 23, 2004

Lerner and Greenberg, P.A.

Post Office Box 2480

Hollywood, FL 33022-2480

Tel: (954) 925-1100

Fax: (954) 925-1101

11. The memory configuration according to claim 8, wherein at least one of said memory cells in said memory matrix includes at least two transistors.

12. The memory configuration according to claim 8, wherein said read/store control apparatus is configured such that the threshold voltage of said further one of said ferroelectric transistors in said memory matrix is increased by applying a drain-substrate voltage to said further one of said ferroelectric transistors in said memory matrix.

13. The memory configuration according to claim 12, wherein said read/store control apparatus is configured such that the drain-substrate voltage is substantially +3.3 volts.

14. The memory configuration according to claim 12, wherein said read/store control apparatus is configured such that the drain-substrate voltage is substantially -3.3 volts.